WAFER BONDING AND LAYER TRANSFER PROCESSES FOR 4-JUNCTION HIGH EFFICIENCY SOLAR CELLS

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ABSTRACT

A four-junction cell design consisting of InGaAs, InGaAsP, GaAs, and $Ga_{0.5}In_{0.5}P$ subcells could reach 1xAM0 efficiencies of 35.4%, but relies on the integration of non-lattice-matched materials. Wafer bonding and layer transfer processes show promise in the fabrication of InP/Si epitaxial templates for growth of the bottom InGaAs and InGaAsP subcells on a Si support substrate. Subsequent wafer bonding and layer transfer of a thin Ge layer onto the lower subcell stack can serve as an epitaxial template for GaAs and $Ga_{0.5}In_{0.5}P$ subcells. Present results indicate that optically active III/V compound semiconductors can be grown on both Ge/Si and InP/Si heterostructures. Current-voltage electrical characterization of the interfaces of these structures indicates that both InP/Si and Ge/Si interfaces have specific resistances lower than $0.1\,\Omega cm^2$ for heavily doped wafer bonded interfaces, enabling back surface power extraction from the finished cell structure.

INTRODUCTION

Detailed balance theory predicts an improved limiting conversion efficiency via increasing the number of junctions in a cell [1]. This prediction has been verified in functional high-efficiency three-junction cells with $Ga_{0.5}In_{0.5}P$, GaAs, and Ge subcells achieving AM0 efficiencies in excess of 26% [2]. However, extension of the multi-junction cell concept to four or more junctions has been difficult due to subcell current and lattice-matching requirements for monolithically fabricated multi-junction solar cells. Efforts have been made to utilize InGaAsN as a ~1.0 eV direct bandgap subcell lattice matched to GaAs. However, poor performance of the InGaAsN subcell prevents cell efficiency improvements from being realized in four-junction cells that utilize this design [3].

From the perspective of current matching and efficient photon collection a four-junction cell consisting of $Ga_{0.5}In_{0.5}P$, GaAs, InGaAsP, and InGaAs subcells is promising with well-developed growth processes and long lifetimes for these materials. However, the top $Ga_{0.5}In_{0.5}P$/GaAs subcell structure with a lattice constant of 5.66Å and the bottom InGaAsP/InGaAs subcell structure with a lattice constant of 5.8Å are not sufficiently well lattice matched for heteroepitaxial fabrication. Fortunately, wafer-bonding processes allow integration of non-lattice-matched semiconductors by isolating the associated misfit defects to the bonded interfaces. For example, it has been previously proposed to wafer bond a GaAs wafer with a $Ga_{0.5}In_{0.5}P$/GaAs cell structure on top to the top of a InGaAsP/InGaAs subcell structure fabricated on an InP wafer using a Sn bonding layer to ensure low-loss ohmic electric contact between the subcell sections. [4] However, this design suffers from the disadvantage of requiring the use of a complete GaAs and InP wafer in each fabricated cell, increasing the finished cell cost. Additionally, the use of a Sn bonding layer and a complete GaAs wafer leads to shadow losses and undesired top cell photoabsorption in the 1-2μm range, reducing bottom subcell absorption.

Implantation of H^+ or co-implantation of H^+/He^+ to high doses has been shown to exfoliate a thin film (<1 μm) from the implanted substrate to a support substrate following bonding and annealing. Importantly, this technique has been proven successful for InP, GaAs, and Ge [5]. Additionally, hydrophobic direct wafer bonding has been shown to leave an atomically abrupt, covalently bonded interface allowing for ohmic electrical contact between bonded materials [6]. A proposed four-junction cell design utilizing wafer bonding and layer transfer materials integration processes is shown in Fig. 1. This design utilizes hydrophobic wafer bonding and H-induced layer transfer to bond thin films of InP to Si support substrates to serve as epitaxial templates for growth of InGaAsP/InGaAs subcell structures while allowing low-loss power extraction from the back surface of the Si substrates. On the top of the bottom subcell structure a thin n^+InP layer would be grown to serve as a bonding surface

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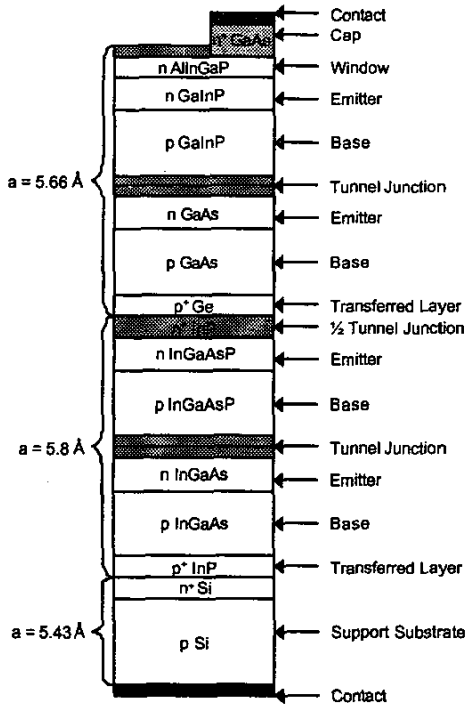

Fig. 1. Schematic of the proposed wafer bonded four-junction solar cell

for bonding and layer transfer of a thin p^+Ge film. The Ge transferred layer would then serve as an epitaxial template for the $Ga_{0.5}In_{0.5}P$/GaAs subcell structure. The p^+Ge/n^+InP interface would once again allow low-loss power transmission through the cell structure. Table 1 summarizes the projected device performance at 1xAM0 illumination assuming 80% transmission of the 1-2 μm wavelengths to the bottom cells. The pracitcal efficiency estimate based on an assumed loss of 15% of the total efficiency to series and shunt resistance effects in the structure is 35.4% at 1xAM0 and 39.8% at 15xAM0 with actual device efficiencies and bandgaps of the bottom subcell structure determined by the spectral transmission through the top subcell structure.

By using wafer bonding and layer transfer processes to fabricate four-junction solar cells, low-cost, mechanically robust Si substrates can be utilized as support substrates and a single high-cost InP and Ge wafer pair could be used to transfer multiple films by use of a suitable reclaim process.

EXPERIMENTAL

InP/Si heterostructures are fabricated from (100) InP wafers implanted with either H^+ or co-implantation with H^+/He^+. H^+ implantation is performed at 80keV to a dose of $2x10^{17}cm^{-2}$. Co-implantation is performed with H^+ at 80keV to a dose of $1x10^{17}cm^{-2}$ and He^+ at 115keV to a dose of $1x10^{17}cm^{-2}$. Ge/Si and Ge/InP heterostructures are fabricated from (100) Ge substrates implanted with H^+ at 80keV to a dose of $1x10^{17}cm^{-2}$. Following ion implantation both Ge and InP are rendered strongly hydrophobic.

Both the implanted and Si support substrates are coated with photoresist to protect the bonding surface from scratches and particles. The substrates are then cleaved into ~1cm^2 samples. The photoresist is removed and the sample is ultrasonic cleaned with acetone and methanol followed by a DI water rinse to leave a smooth particle free surface. This surface is then rendered hydrophobic with 5-10% HF solution. Care is taken when preparing the sample surface to maintain a surface roughness less than 5Å-rms as measured by atomic force microscopy (AFM) to ensure intimate contact between the bonding surfaces. Bonding between the clean hydrophobic implanted sample and support sample is then initiated by slight pressure at room temperature. The room temperature bonded samples are then annealed to a temperature of ~225°C under a pressure of ~0.5MPa to initiate H-induced layer exfoliation and layer transfer.

RESULTS AND DISCUSSION

The wafer bonding and layer transfer process described above has been applied to the successful fabrication of

Tab. 1. Subcell structure and efficiencies for four-junction solar cell design .

	Bandgap (eV)	Theoretical Efficiency @ 1xAM0	Practical Efficiency @ 1xAM0	Practical Efficiency @ 15xAM0
$Ga_{0.5}In_{0.5}P$	1.82	19.6 %	-----	-----
GaAs	1.42	12.1 %	-----	-----
Top Subcells	-----	*31.7 %*	*27.0 %*	*30.3 %*
InGaAsP	1.05	7.1 %	-----	-----
InGaAs	0.72	2.8 %	-----	-----
Bottom Subcells	-----	*9.9 %*	*8.4 %*	*9.5 %*
Total	-----	***41.6 %***	***35.4 %***	***39.8 %***

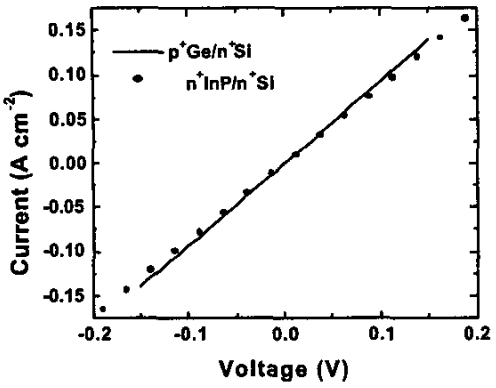

Fig. 2. Interfacial resistance of InP/Si and Ge/Si wafer bonded interfaces.

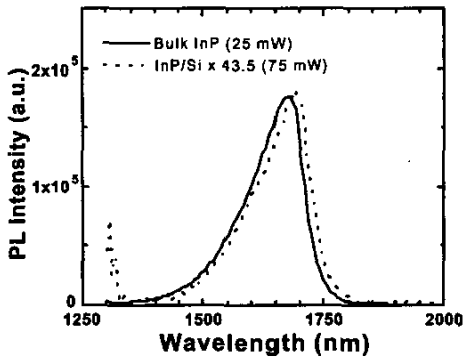

Fig. 3. InGaAs DH PL spectra from a bulk InP control wafer and an InP/Si wafer bonded heterostructure.

~1cm^2 Ge/Si, Ge/InP, and InP/Si heterostructures. The application of pressure during the layer splitting anneal suppresses the tendency for trapped gas to form bubbles at the interface. The as-cleaved surface of the InP exhibits 9-10nm-rms roughness and Ge layers exhibits 10-20nm-rms roughness depending on the miscut of the implanted wafer from the (100) surface as measured by AFM.

The electrical properties of both InP/Si and Ge/Si bonded interfaces were studied to verify that low-loss ohmic electrical contact can be achieved. The band offsets and Fermi level positions of the dissimilar materials in wafer bonded pairs indicate that a potential barrier at the bonded interface can be expected. To prevent this barrier from causing rectification or high resistances at the interface, heavily doped structures were fabricated. The InP/Si interface was studied using an n$^+$InP bulk substrate doped to 2x10^{17}cm^{-3} and bonded to a n$^+$Si substrate doped to 1x10^{19}cm^{-3}. The Ge/Si interface was studied using a p$^+$Ge bulk substrate doped to 1x10^{19}cm^{-3} to bonded an n$^+$Si substrate doped to 1x10^{19}cm^{-3}. Al contacts were defined by evaporation on both of the bonded wafer pairs. Both the InP/Si and Ge/Si samples showed ohmic interfacial electrical properties with interfacial specific resistances of <0.1 Ωcm^2 for each sample (see Fig. 2). Furthermore, the measured resistance was dominated by probe tip to metal contact resistance that could not be accurately extracted from the measurement. The I-V properties of Ge/Si samples with up to 15° azimuthal twist were studied revealing no observable change in the interfacial resistance of the samples. Thus, repeatable tunnel junction contact is possible for the Ge/Si systems.

The suitability of as-cleaved InP/Si wafer bonded heterostructures for MOCVD heteroepitaxy has been investigated by growing an InGaAsP/InGaAs/InGaAsP double heterostructure (DH). Photoluminescence (PL) spectra were observed at room temperature with a 1064nm wavelength probe in a 10μm diameter spot. PL intensity for a probe power of 25mW in a DH grown on a bulk InP wafer was compared to PL intensity for a probe power of 75mW in a DH grown on a wafer bonded InP/Si heterostructure revealing reduced InGaAs band edge emission intensity in the InP/Si sample relative to the control (See Fig. 3).

MOCVD triple-junction solar cell structures have been grown on as-cleaved Ge/Si wafer bonded heterostructures to assess the suitability of this system as an epitaxial template for the growth of triple-junction solar cells on Si support substrates [7]. This system illustrates the as-cleaved Ge surface suitability for growth of the top two subcells of the proposed four-junction device. PL spectra were observed at room temperature using a 457nm wavelength probe in a 50μm diameter probe spot at a probe power of 25mW. PL spectra of the GaAs cap layer in the triple-junction structure shows comparable GaAs band edge emission intensity between a layer grown on Ge/Si and a layer grown on a bulk Ge control (see Fig. 4a). Selective etching was used to expose the $Ga_{0.5}In_{0.5}P$ subcell, and PL spectra of this layer showed comparable $Ga_{0.5}In_{0.5}P$ band edge emission intensity between the two layers (see Fig. 4b) [7].

Both InGaAs grown on InP/Si and $Ga_{0.5}In_{0.5}P$ grown on Ge/Si show slight bandgap shifts to longer wavelengths compared to control structures grown on bulk substrates. This effect may be attributable to ordering of the group III sub-lattice or to strain in the grown films arising from the coefficient of thermal expansion mismatch of the grown layers and the Si support substrate. Fig. 5 shows the thermal expansions of GaAs [8], InP [9], Ge [8], and Si [8] through the temperature range of interest for wafer bonding and subsequent MOCVD growth. Relaxed GaAs or InGaAs grown by MOCVD at temperatures up to 900K should lead to a tensile strained layer at room temperature. This could lead to bandgap shifts of the subcell materials at the operating temperature.

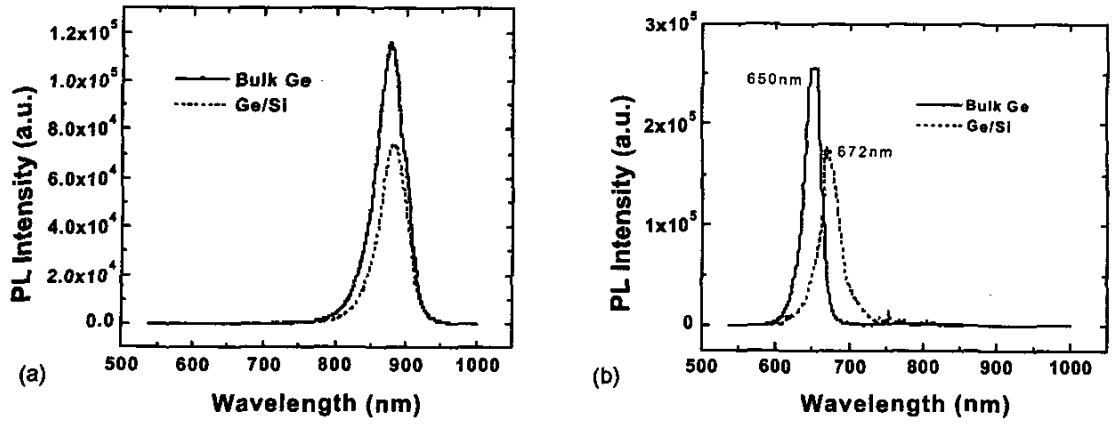

Fig. 4a-4b. GaAs PL spectra from the GaAs cap layer of a triple-junction solar cell (a). $Ga_{0.5}In_{0.5}P$ PL spectra from the $Ga_{0.5}In_{0.5}P$ subcell of a triple junction solar cell (b).

In addition to the room temperature properties of MOCVD grown structures, thermal mismatch may affect the high temperature MOCVD growth on wafer-bonded heterostructures. With growth temperatures well above the bonding and layer transfer temperatures the transferred layer will be in compressive strain, increasing the misfit between the transferred layer and the MOCVD grown structure. One way to minimize such an effect is to initiate bonding at a temperature higher than room temperature but lower than the blistering temperature for the H-implanted substrate.

CONCLUSIONS

Active $Ga_{0.5}In_{0.5}P$, GaAs, and InGaAs layers have been grown on wafer bonded epitaxial templates. Ohmic low-loss electric contact has been demonstrated between InP/Si and Ge/Si wafer bonded structures. Thus, use of wafer bonded heterostructures appears to be feasible for fabrication of a proposed four-junction solar cell utilizing wafer bonding and layer transfer processes shows promise for achieving efficiencies in excess of 35.4% at 1xAM0 and 39.8% at 15xAM0. Importantly, wafer bonding and layer transfer processes will enable this structure to be fabricated on a low cost, mechanically robust Si substrate.

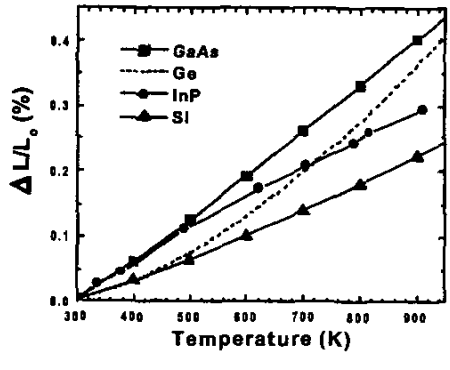

Fig. 5. Thermal expansion for InP, Ge, GaAs, and Si over the temperature range for wafer bonding and MOCVD growth.

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